

Keynote Address

***The Increasing Role of Dielectric Layers
in Flip-Chip and Wafer Level Packaging***

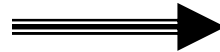
***Bob Hubbard
Lambda Technologies, Inc.***

What; more layers?!

- ❑ The “planarization” of packaging
- ❑ The drivers to add layers
- ❑ Planar package constructions
- ❑ An update on polymer dielectric layers
- ❑ Material characteristics and reliability
- ❑ Changing demands on flip-chip
- ❑ Alternatives and directions

The Planarization of Transistors

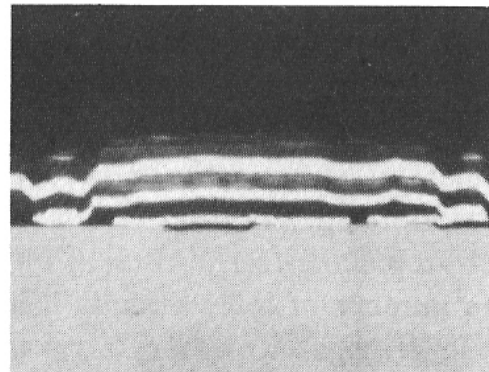
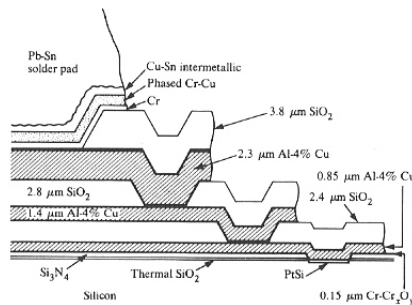
- From vertically assembled and wired transistors to monolithic layers of semiconductors



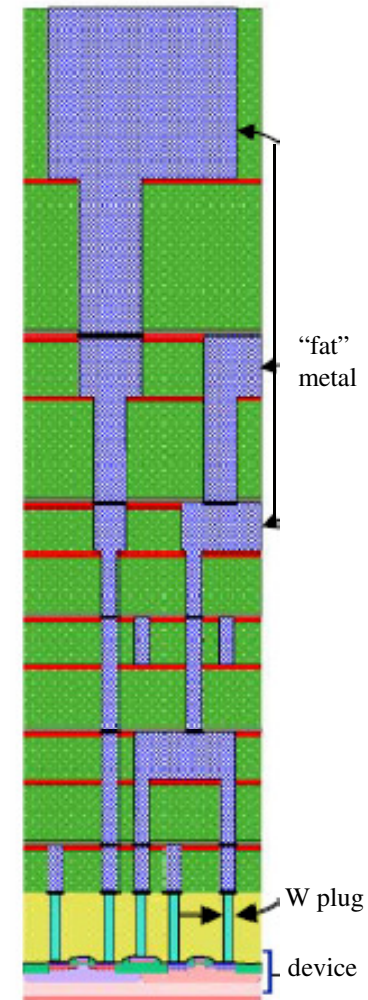
from Jack Kilby's notebook

The Planarization of Integrated Circuits

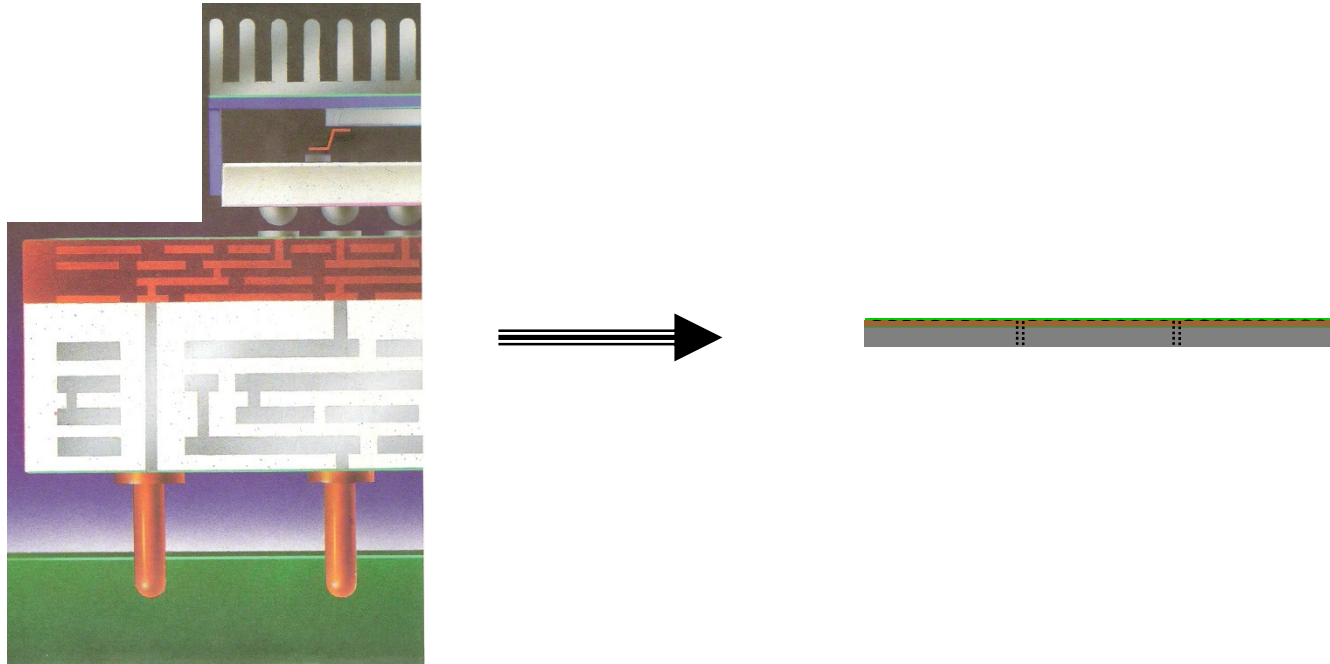
- Cu wiring with SiO₂ dielectric layers (1982!)



- Cu wiring with low-k dielectric layers (2000)
- Now 4 layers for DRAM, 9 layers for logic



The Planarization of Packaging



- Planarization: adding dielectric and metal layers for interconnects

The Planarization of Systems

□ The component list is getting longer:

- passives
- sensors
- power
- connectors
- optics
- MEMS
- thermal
- video
- RF



Integration will come
with new organic and
composite materials

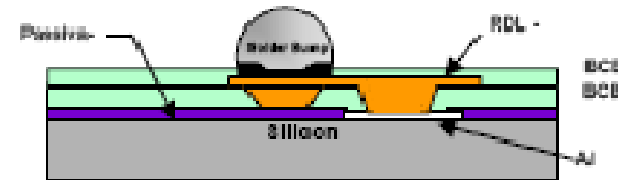
(this is a much slower process
outside the silicon infrastructure)

From Passivation to Wafer Level Packaging

- Stress buffer / passivation layers
 - Silicon nitride for moisture and halogen protection (passivation)
 - Polymer layer for stress relief from encapsulation/molding

- One more re-distribution layer (RDL)
 - Transition from WB to bumps
 - Transition from periphery to array

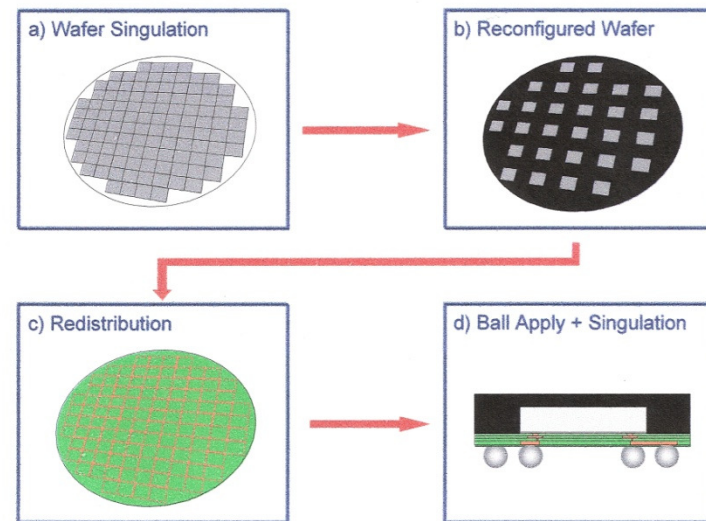
- Two – eight interconnection layers (WLP)
 - Moderate (50-200) I/O devices
 - Fan-out beyond IC borders



A Universal Package?

□ The old “chips first” re-visited

- Assemble an array of tested dice
- Protect the die back and sides with encapsulant
- Add layers of interconnect to die faces
- Fan-out pads for high density chips
- Bump and dice



courtesy Infineon Technologies

The Drivers of Change

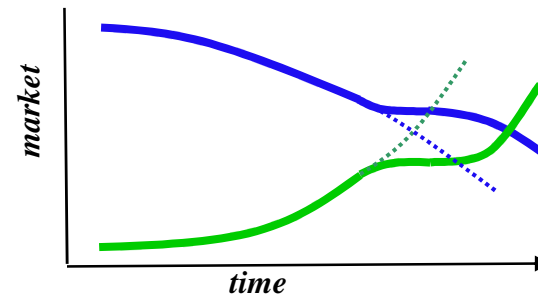
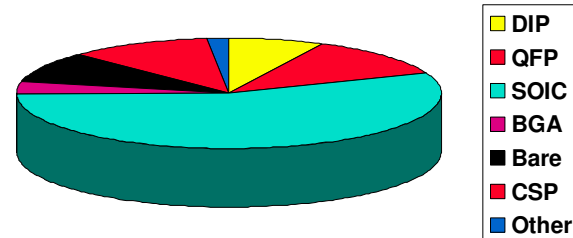
- Cost
 - Wafer processes are bulk
 - Fewer total process steps
 - Additional costly substrate not necessary
 - Test at wafer or known-good-die approaches add cost
- Thickness
 - Thin is in! (Motorola RAZR, Motorola Q, Samsung A900)
 - Stacked dice were already forcing wafer thinning to 50 um
- Reliability
 - Fewer material interfaces
 - Fewer separate parts to protect
 - Fewer adhesive joints

The Death of Wire-Bonding?

- No.
 - The majority of devices will continue to be wire-bonded for some time

 - All existing technologies fight replacement

 - Can DDR3 and DDR4 be wire-bonded?
 - Two studies; two answers



Dielectric Material Properties

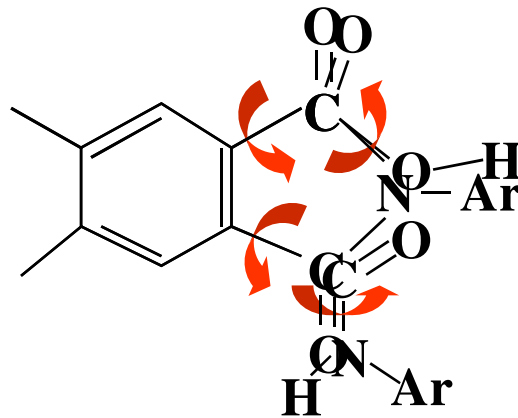
Changing Material Property Needs - WLP

- Stress buffer layer needs before 2000
 - High temperature stability for reflow
 - High elongation for die stresses
 - Low outgassing
 - Adhesion to die

- Current multilayer RDL and WLP
 - High temperature stability for multiple processes and reflow
 - High elongation for die and multi-layer stresses, and shock testing
 - Chemical resistance to develop solvents and etchants
 - Water based development for the environment
 - Lower thermal budget for curing (die yield)
 - Low temperature curing for sensitive devices (<200°C)
 - Fast curing for multiple layer throughput (>50 WPH)
 - Adhesion to previous layer

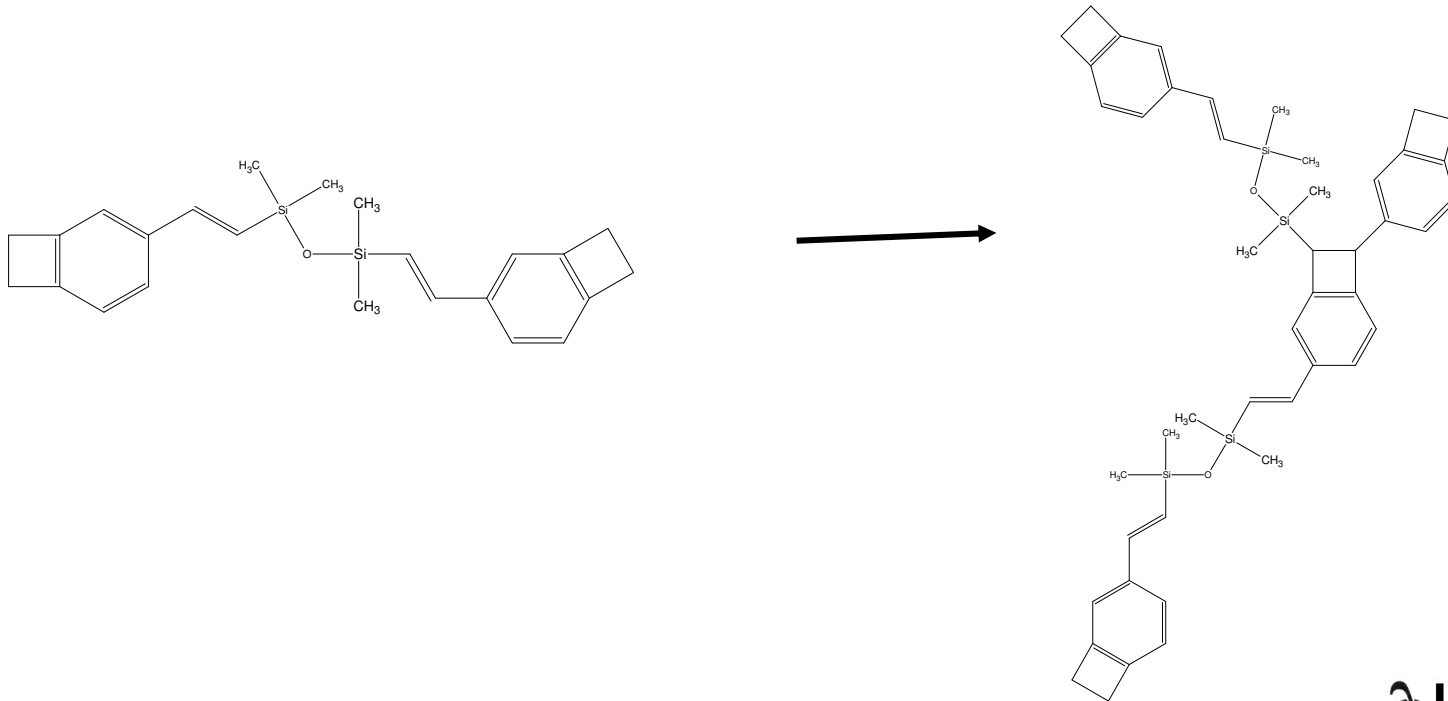
Dielectric Material Properties - PI

- Polyimides for stress buffer layers
 - High elongation, low modulus, planarizing, “soft” coating
 - High temperature stability, chemically resistant, α particle barrier
 - Photo-sensitive, solvent based development, linear
 - High temperature, long cure (350°C, 4 hrs), 2% moisture retention



Material Properties - BCB

- ❑ Benzocyclobutene (Cyclotene) for re-distribution
 - Low elongation, low dielectric constant, planarizing, “hard” coating
 - High temperature stability, oxygen sensitive, α particle barrier
 - Photo-sensitive, solvent based
 - Moderate temperature, long cure (250°C , 5 hrs)



Material Properties - Epoxies

- Epoxy “hybrids” for wafer level packaging
 - Low temperature, shorter cure (175-190°C, 3 hrs)
 - Low elongation, high modulus, “hard” coating
 - Lower temperature stability, chemically resistant
 - Photo-sensitive, solvent based, resin or film
 - Cross-linked
 - Thermal processing affects mechanical properties

Dielectric Material Comparisons

- Choices depend on number of layers, low-k dielectric layers, type of device, device properties, type of application, throughput, size of wafers, technology node (45 nm?), environment, etc.

	Tg	Cure time*	Cure Temp	Elong.	Process	Stability
PI	300	5 hr	350	80%	Solvent	>400°C
PBO	300	5 hr	380	100%	Water	>400°C
BCB	280	8 hr	250	5%	Solvent	>300°C
Epoxy	200	3 hr	190	4%	Solvent	?

* customer variation can be significant

Is Your Dielectric Layer Really Cured?

- Polymer dielectrics must be highly cured to have good adhesion

- Many dielectric layers now in use are not highly cured
 - Historical use of 180°C polyimide coatings
 - Epoxy based microvia boards with un-cured resin may crack internally after reflow processes
 - Shifting modulus, CTE, elongation affects layer stresses
 - “Standard” processes are not always full cure
 - DSC or FTIR will show extent of cure until about 90%
 - TMA or DMA will provide Tg, which is more cure sensitive

 - How cured is cured enough?

Epoxy Adhesive Films

- ❑ Flip-chip under-fill, CSP/BGA under-fill

- ❑ Process drivers

- Fast flow
- Fast cure
- Fine pitch
- Self filleting
- Flux compatible
- Long pot-life

- Reliability drivers

- low warpage
- thermal stability
- adhesion
- low stress
- large die
- high I/O

- ❑ Two new drivers

- Higher reflow temperatures (no-lead)
- Fragile low-k dielectric layer(s)

Material Supplier Directions

- Wafer Dielectrics
 - Faster and lower temperature cure of PI and PBO
 - New chemistries and formulations
 - Epoxy “hybrids” and photo-resists
 - Lower temperature cure

- Flip-chip underfills
 - Lower shrinkage, lower stress
 - Compatibility with low-k dielectrics
 - Lower Tg + lower modulus but low CTE

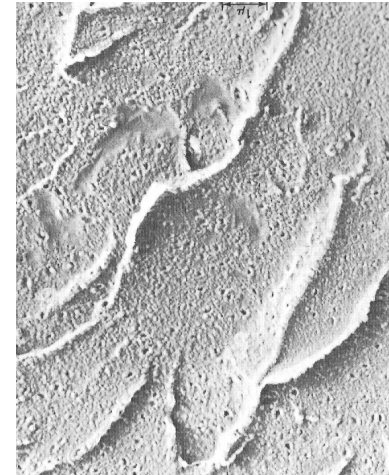
- New families of materials
 - Packaging consortia all have chemical partners
 - Focus is on mechanical properties (CTE, E', Tg, etc.)

The Dielectric Curing Process

(for cross-linked polymers)

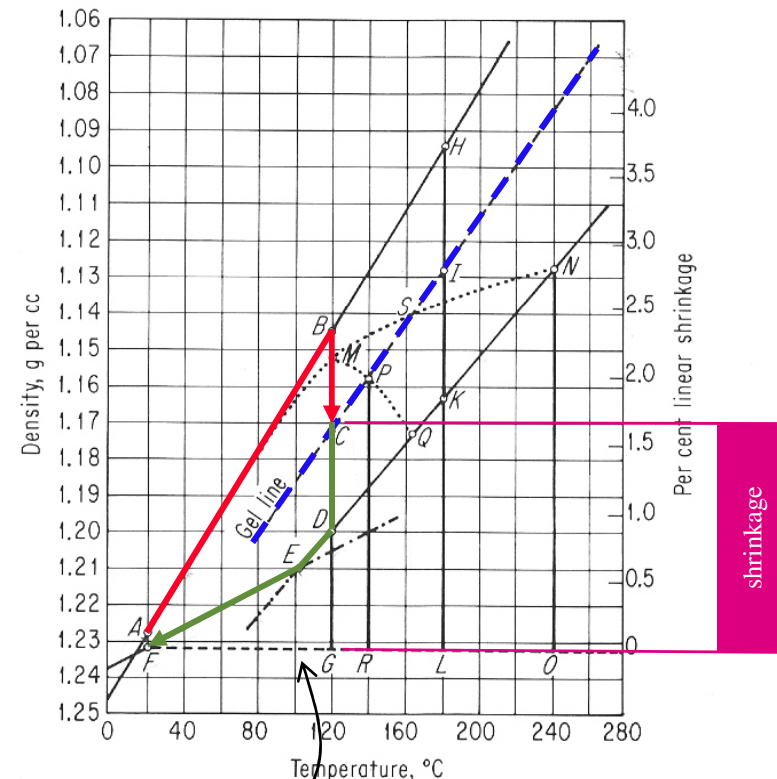
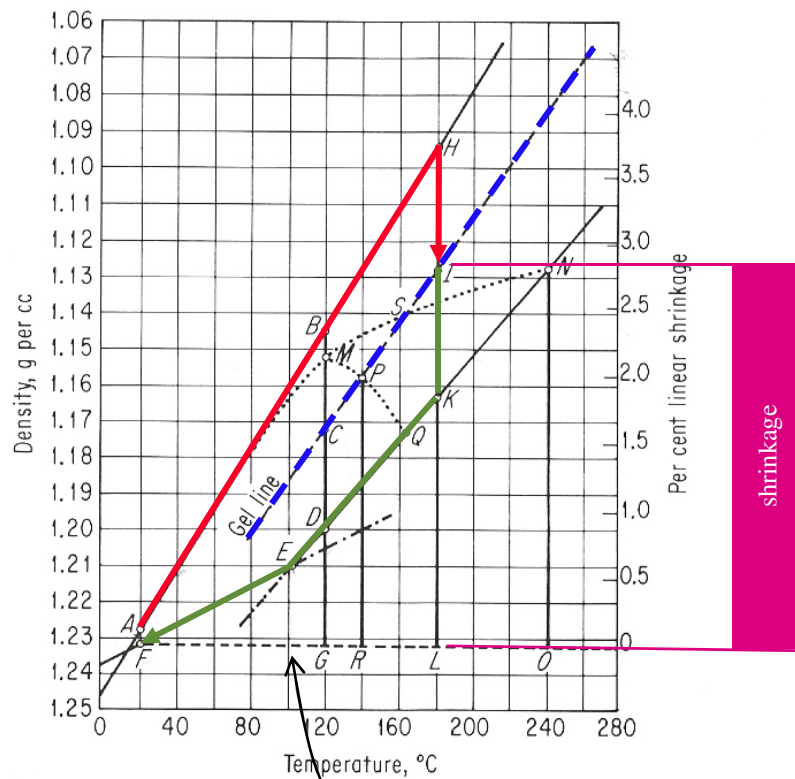
“Liquid State” and “Solid State” Curing

- Low temperature cure step:
 - majority of shrinkage occurs in liquid state
 - size of agglomerates determined by cross-link density
 - “network” extent of cure constrained by cross-link density
 - gelation: change from liquid to solid state curing
 - entrapment of uncured molecules in “network”
- High temperature cure step
 - continued growth of agglomerates
 - completion of cross-linking if possible
 - some cross-linking physically blocked
 - curing of entrapped molecules
 - thermal and chemical resistance enhanced
 - yield strength and adhesion enhanced
 - continued shrinkage during cooling



Total shrinkage (not simply highest temperature)

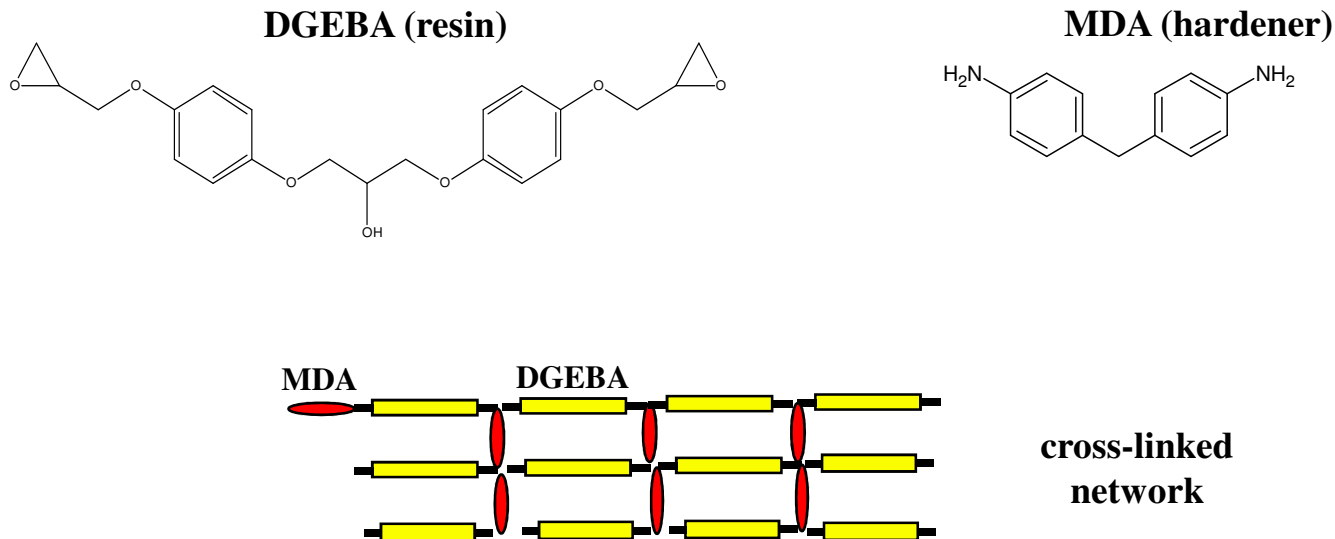
1. Liquid state shrinkage (>50%)
2. Solid state shrinkage (difference between gel and RT)



Note: The T_g of both materials is the same.

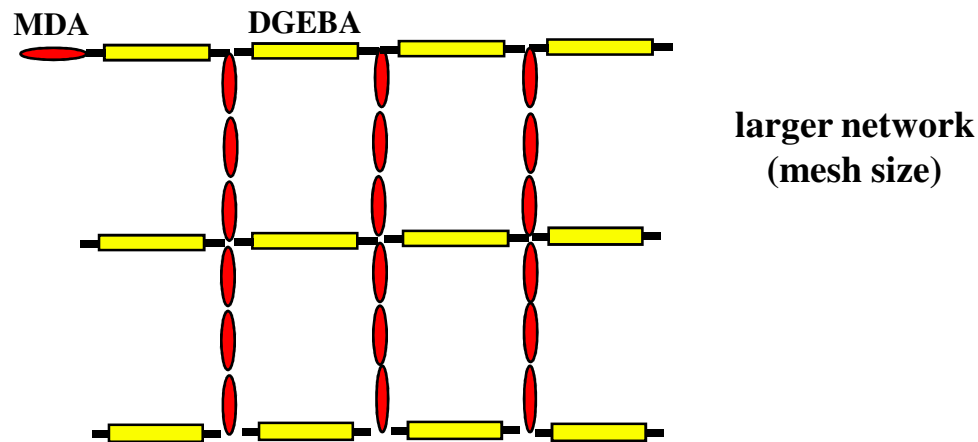
Closer Look at Cross-linking

- ❑ PBO dielectric layers for WLP
- ❑ Epoxy dielectric layers and adhesives for flip-chip
- ❑ Example of epoxy cross-linking:



Change the Curing Process?

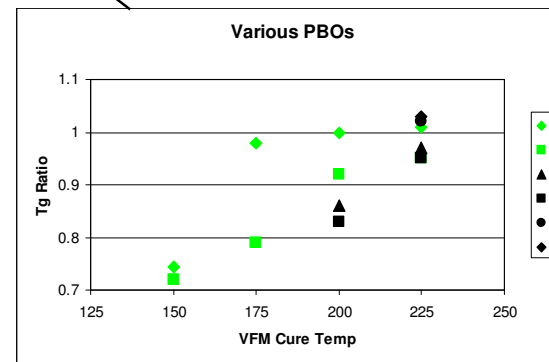
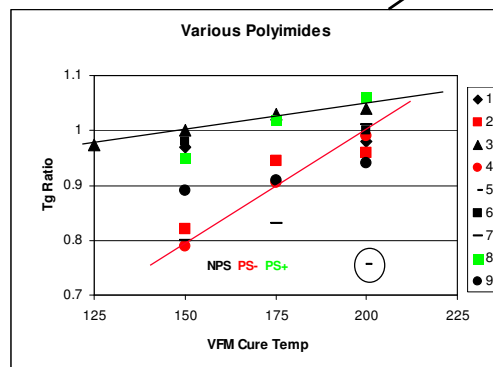
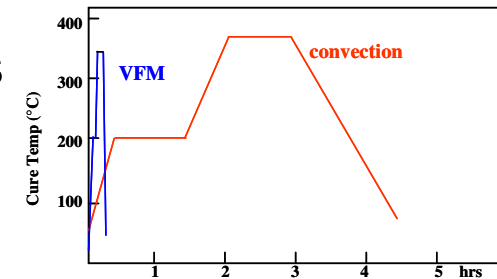
- ❑ Lower the cure temperature, for example
- ❑ Change the balance of low and high temperature steps



- ❑ Benefits:
 - increases elongation, toughness, resistance to crack propagation
 - decreases shrinkage, tension and compression modulus, brittleness

Curing with Microwaves

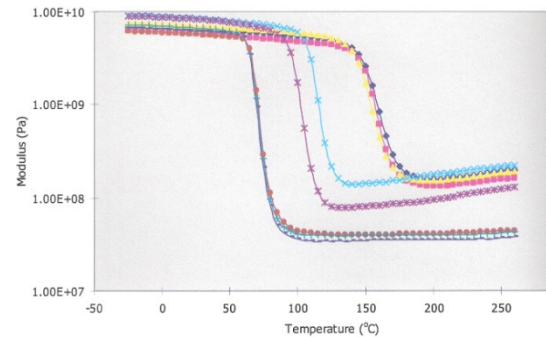
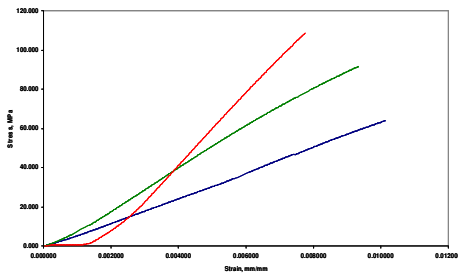
- Obviously faster curing: 5 hours to 15 minutes
- Lower temperatures for PI and PBO:



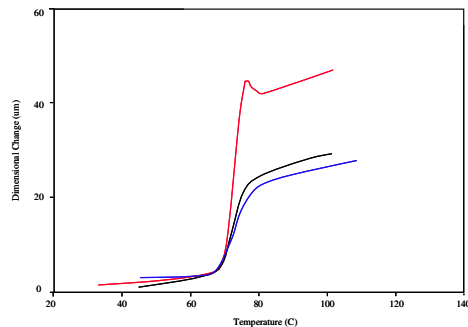
350°C – 5 hrs \implies 175°C – 1 hr

Modified Properties with Microwaves

- Tg must remain the same (adhesion, thermal stability)
- Lower modulus with low temperature cure



- Raise or lower the CTE with cure profile



Profile	MW	Conv	MW
CTE (ppm/C)	44	68	109

Summary

- ❑ As planarization continues
 - dielectric materials and processes become more critical

- ❑ Material properties affect package reliability

- ❑ Material requirements continue to change
 - new chemistries and new processes

Change Grinds On!

