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Warpage Reduction for Flip-Chip Under-Fill

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Industry Movement to Higher Stress

❑ Stress increases for:

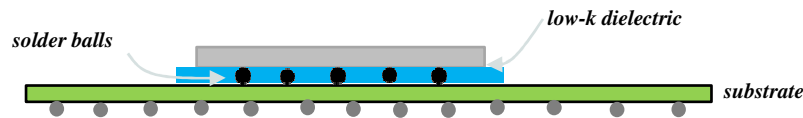
- larger wafers
- thinner wafers
- wafer bonding/stacking
- more wafers per stack
- more brittle dielectrics (low k)
- larger dice
- finer bump pitches
- thinner packages (coreless)
- sensitive structures (sensors)
- sensitive devices
- increased handling
- more devices per die
- fewer die per wafer

❑ Solutions:

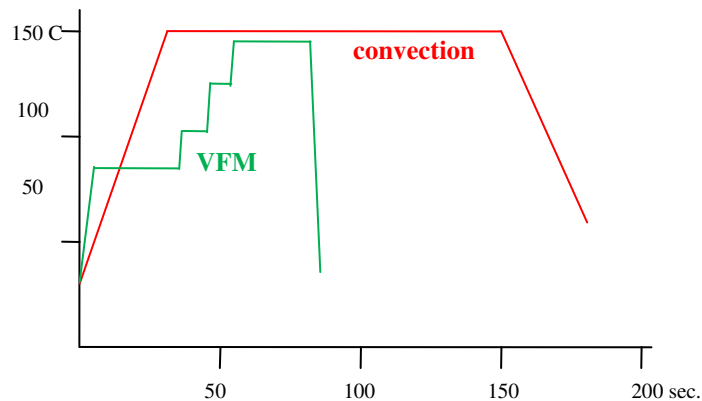
- Design
- Material
- **Process**

Reduced Stress with Microwave Curing

- ❑ Stresses built in can cause latent failures
 - Warped die crack the outer solder balls
 - Warped die crack the interconnect layers
 - Warped thin substrates can't be assembled



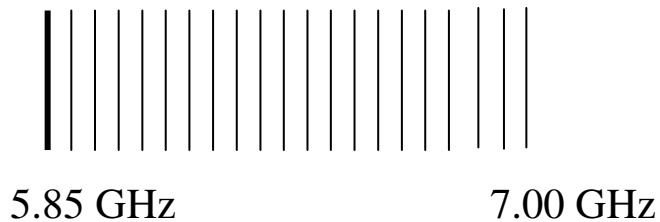
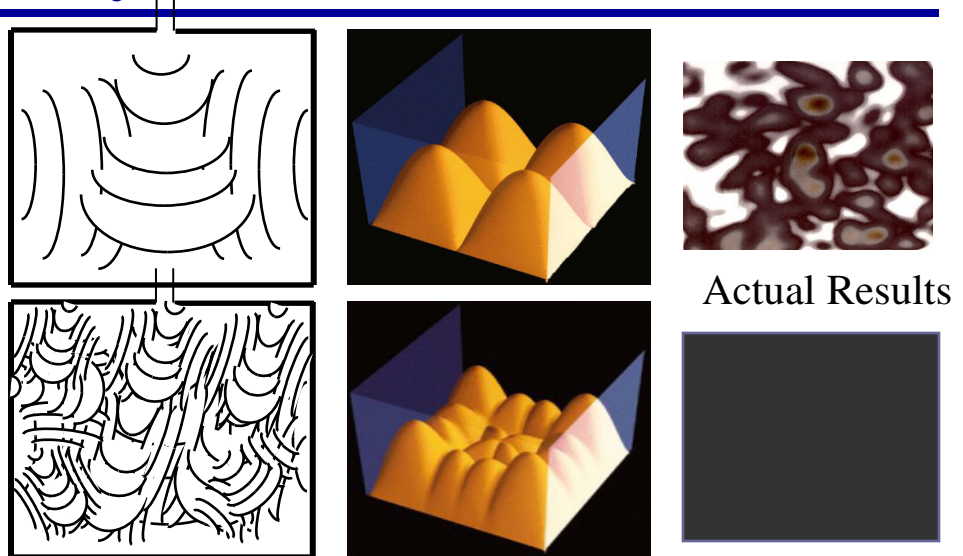
- ❑ Faster and lower temperature under-fill cure = lower stress!



(UF cured to same thermal and mechanical properties)

Why Variable Frequency Microwave (VFM)?

- ❑ Single (fixed) frequency creates spacial nodes of high and low energy distribution
- ❑ Variable Frequency microwaves mix nodes every 25 μ s for uniform energy distribution
- ❑ Multiple scanned frequencies
 - 4096 frequencies, every 0.1 second



$$P_{ave} = \omega \epsilon_0 \epsilon''_{eff} E_{rms}^2 V$$

P_{ave} = Average power dissipated
 ω = angular frequency
 ϵ''_{eff} = dielectric loss factor
 E_{rms} = electric field intensity (rms)
 V = volume of the load

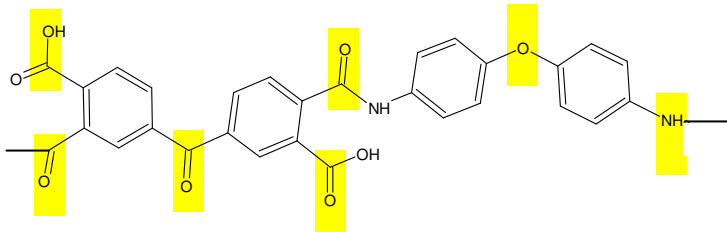
- Since power is proportional to the square of applied field, any non-uniformity is amplified both in scaling up and at the smallest geometries.
- There is no arcing or burning of parts with VFM

Effects of VFM on Semiconductors

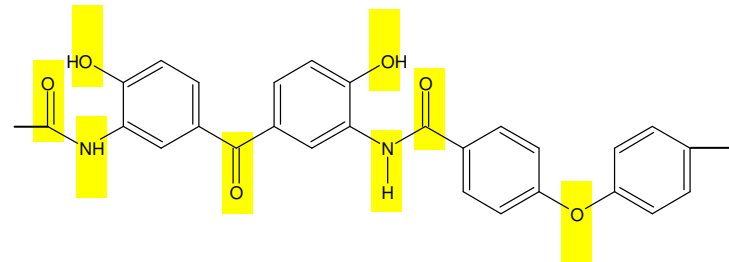
- ❑ VFM does not damage semiconductor devices.
 - Microwave energy is non-ionizing.
 - Activation energies are orders of magnitude below energies of junction alteration.
 - Crystal lattice structure energy too high for microwaves.
 - Voltage levels are below breakdown voltages
 - No arcing or charge build up (short residence time - 25 μ s)

- ❑ Most of the major semiconductor fabs have evaluated VFM:
 - No damage from VFM to devices
 - No change in dopant distribution or localization
 - No effects on memory, logic, or microprocessor devices at least down to 42nm technology
 - VFM used in production processes 24/7 world-wide

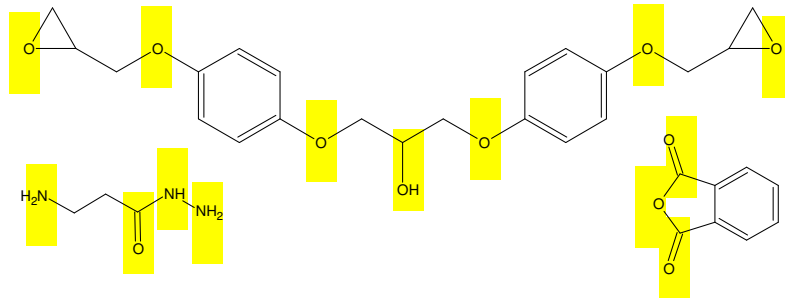
Dipoles in Polymer Resins



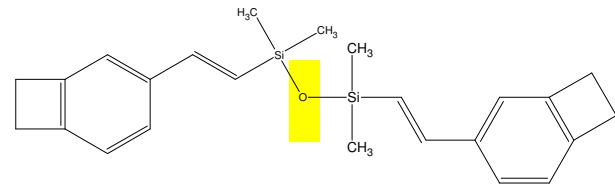
PI



PBO



Epoxy



BCB

Warpage Reduction from Process Optimization?

- Can standard convection be optimized for warpage?
- Is warpage increased with solder reflow at 260°C?
- Established literature on low warpage with VFM
 - Encapsulants and wafer films cured at lower temperatures, faster
 - Lower stress and warpage is a common feature of VFM
- Published data: curing of Henkel FP4527 ¹ and other UF with VFM ²
 - Faster time, lower temperature and 4X lower die warpage
 - Cured UF not taken through additional temperature steps
- Other under-fill chemistries?
- What explains this warpage/stress reduction?

1. Z.Fathi, et.al., Proc. Elect.Pack. Mat. Sci., IX Symposium, MRS, p125, Boston (1997)
2. B. Anderson, et.al., Circuits Assembly, July 1998.

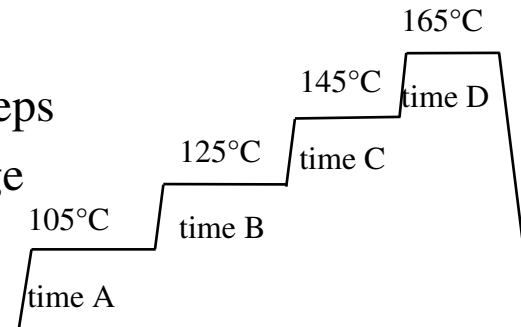
New Low Temperature VFM Under-fill Expts.

- ❑ New study on FP-4527
 - 40mm sq x 0.059 BT boards with solder-mask ($T_g = 155^\circ\text{C}$ by TMA)
 - BT boards pre-baked 165°C for 30 min (eliminate effect of board cure)
 - 20 & 20 mm square silicon die with solder balls (PBGA)
 - Shadow Moire' patterns measured on die top and bottom of board
 - Co-planarity of die and BT substrate measured before heating
- ❑ Evaluate warpage after three 260°C solder reflow cycles
- ❑ Optimization of convection cure profiles
- ❑ Different UF chemistry: "Hybrid"
- ❑ Evaluate thin die and core-less boards

VFM Curing of FP-4527

Can VFM cure profiles reduce warpage even AFTER REFLOW

- **Convection standard: 30 min @ 165°C**
- Cure profile DOE using programmed multi-steps
 - Find temperatures that affect final warpage
 - Ramp rates: 30-60 °C/min
 - Total cycle time faster

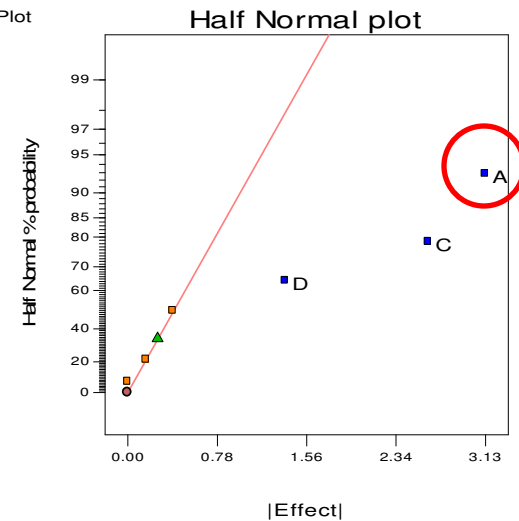


Effect of temperature steps:

- **105°C strongest effect on warpage**
- **105°C (40min) + 145°C (8min)**
best combination for Si & BT
- No effect of fast ramp rates
- More improvement? Longer 105°C time

DESIGN-EXPERT Plot
W(cured+3X)Si

A: time@105
B: time@125
C: time@145
D: time@165

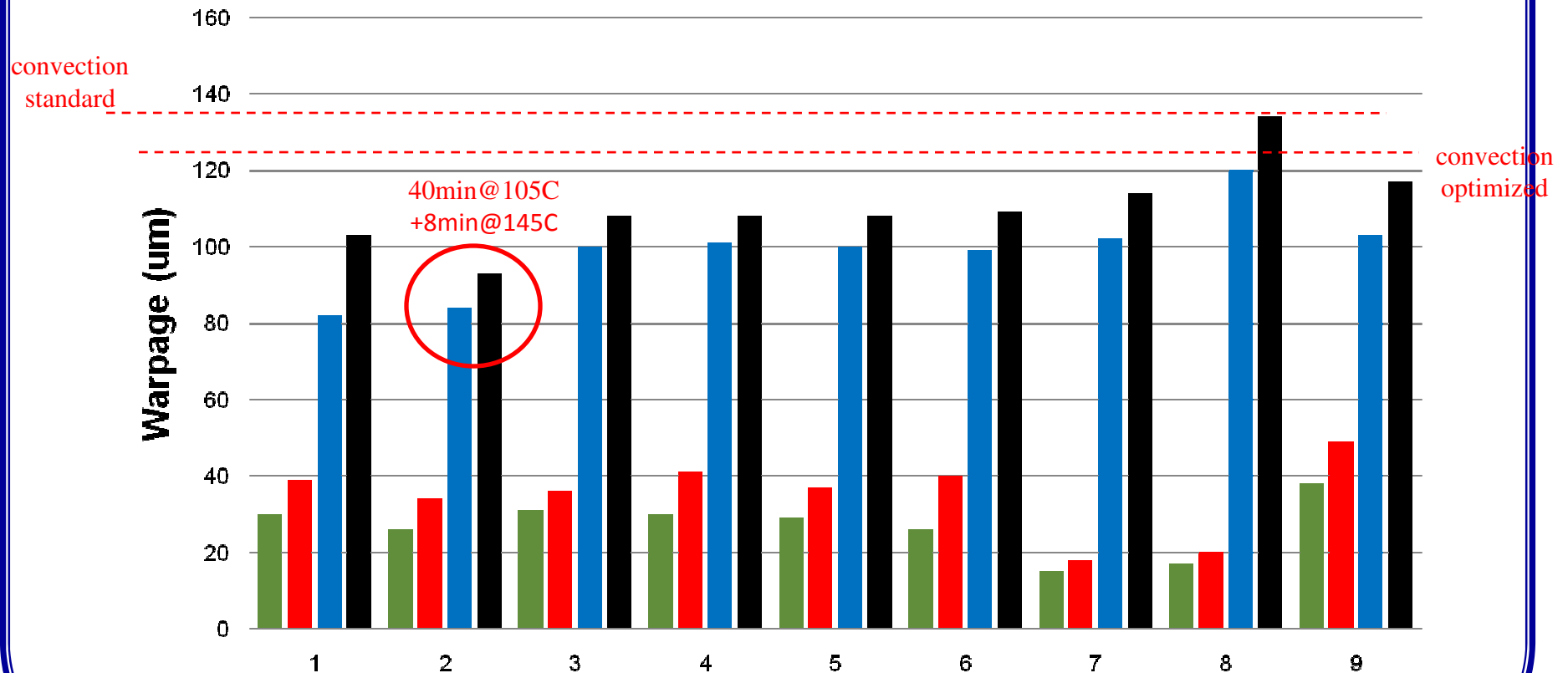


Co-planarity of BT with VFM UF cure

□ “1-9” are multi-step DOE profiles

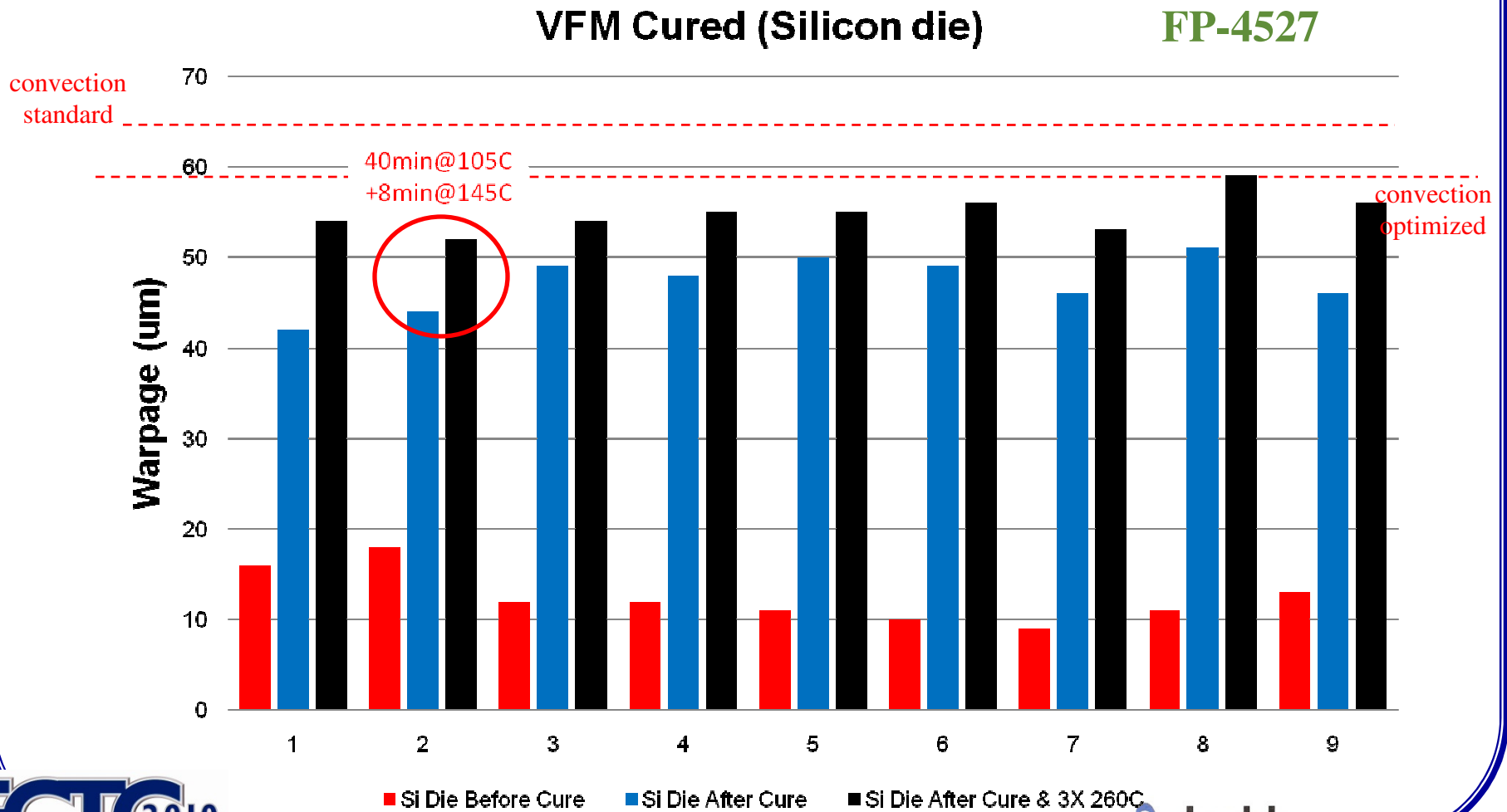
VFM Cured (BT Substrates)

FP-4527



Si Die warpage with VFM UF Cure

☐ “1-9” are multi-step DOE profiles



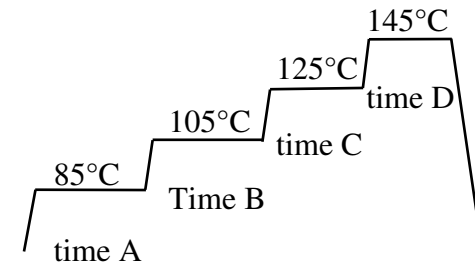
Confirmation Runs: FP-4527

- Convection (standard): 30min ramp to 165°C + 30min@165°C
- Convection (optimized): 45min ramp to 145°C + 22min@145°C
- VFM: 40min@105C + 8min@145C
 - This is DOE Run#2 which was not optimized
- 12 parts each; BT was 59mils thick, die were 20mm on a side
- Co-planarity to edges measured in microns with Shadow Moire'

	BT (after cure)	BT (3X reflow)	Si (after cure)	Si (3X reflow)
Convection (std)	135	114	59	63
Convection (opt)	124	120	58	60
VFM	95	103	45	53
Std. dev.	13.3	12.5	1.6	1.6
Change	- 24%	- 14%	- 24%	- 13%

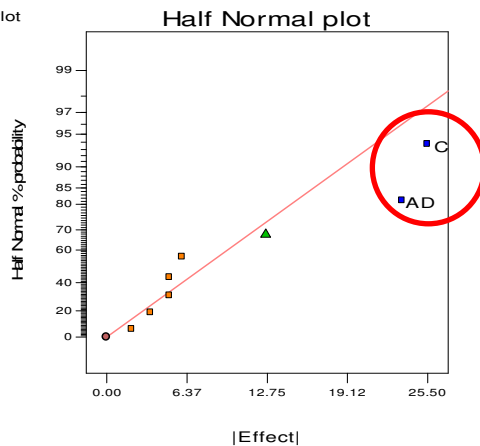
VFM Cure of Hybrid UF

- ❑ Standard oven process cure: 120 min @ 150°C
- ❑ DOE for warpage with VFM cure
 - Two way interaction of **85°C & 145°C**
 - Smaller effect of 125°C



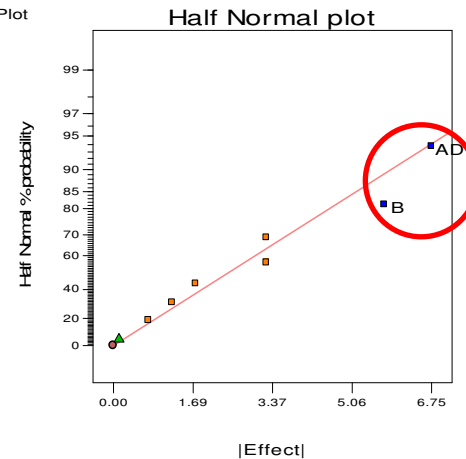
DESIGN-EXPERT Plot
BTWarp(ref low)

A: Time@85
B: Time@105
C: Time@125
D: Time@145



DESIGN-EXPERT Plot
SiWarp(ref low)

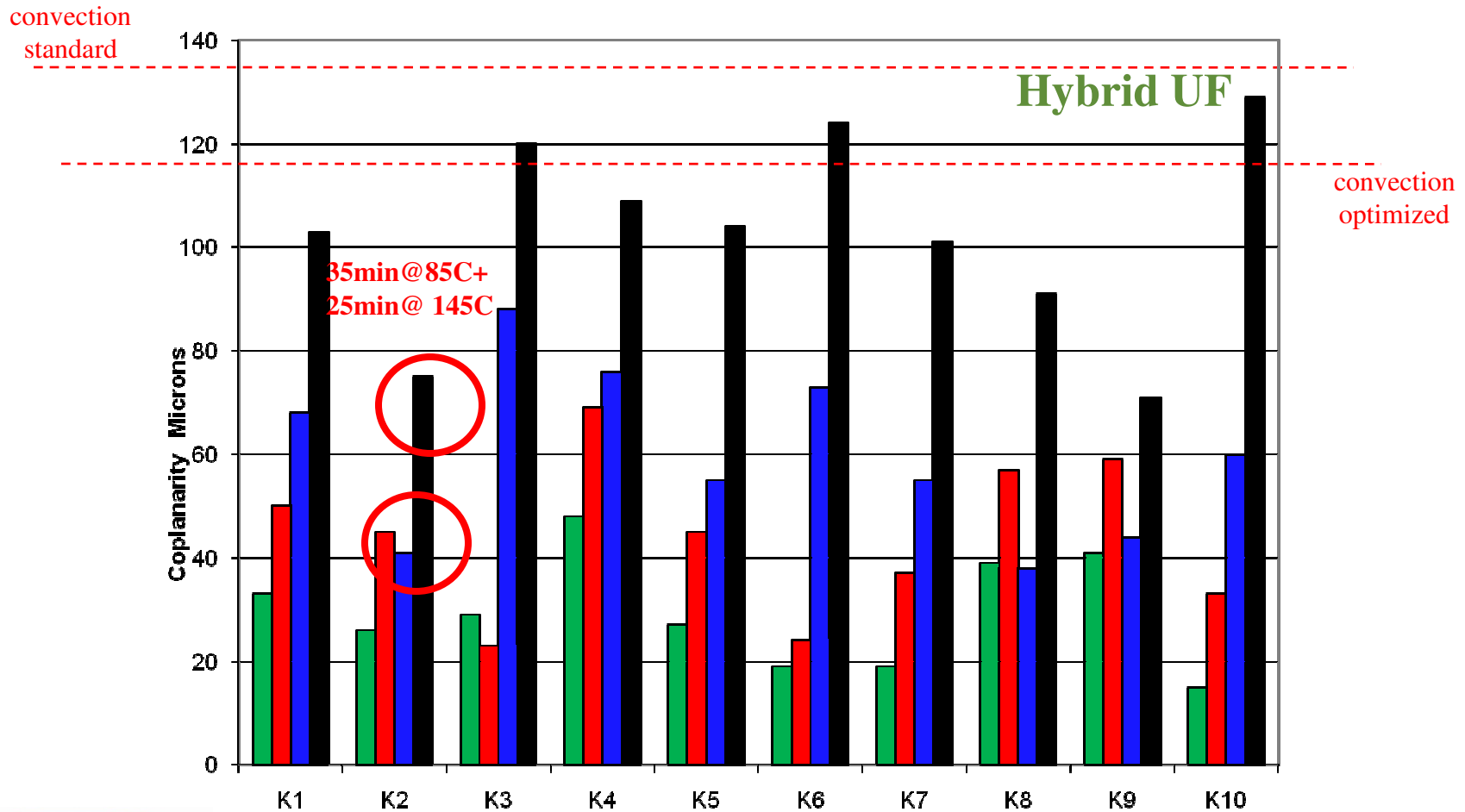
A: Time@85
B: Time@105
C: Time@125
D: Time@145



- ❑ DOE for warpage with standard convection oven
 - Optimum: 30min@85C+30min@105C+30min@125C+30min@145C

Board Warpage of VFM Cured Hybrid UF

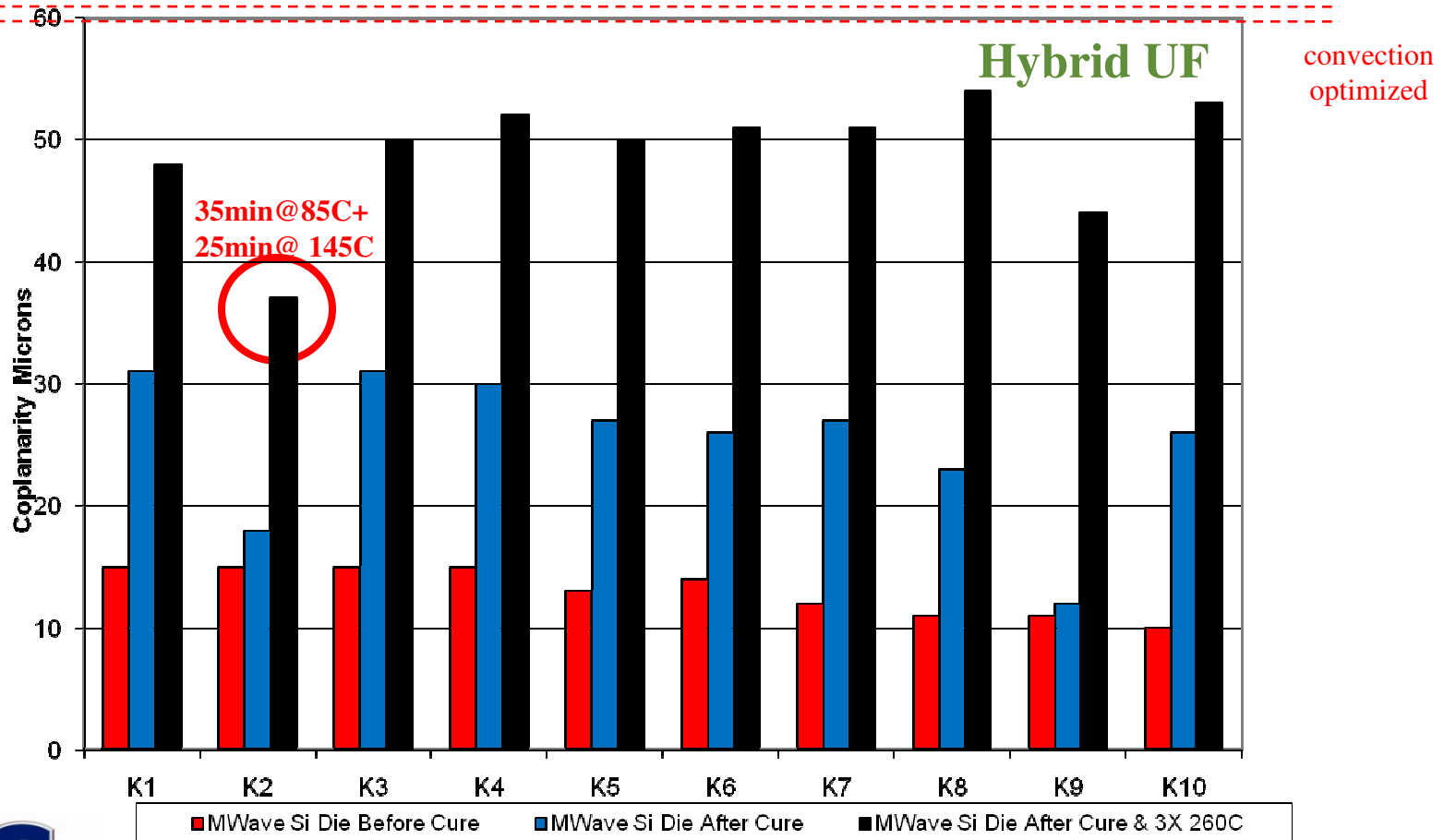
☐ “K1-K10” Multi-step profile runs



Die Warpage of VFM Cured Hybrid UF

☐ “K1-K10” are multi-step DOE runs

convection
standard



Confirmation Runs: Hybrid Epoxy UF

- ❑ Convection (standard): 35min ramp to 150°C + 120min@150°C
- ❑ VFM: 35min@85C + 5min@105C + 5min@125C + 25min@145C
 - This is DOE Run#2 which was not optimized
 - Predicted from Run#2 shown as "VFM (DOE)" with 20 mm on a side
- ❑ 10 parts each; BT was 60 mils thick, die were only 15 mm on a side
- ❑ Co-planarity to edges measured in microns with Shadow Moire'

	BT (after cure)	BT (3X reflow)	Si (after cure)	Si (3X reflow)
Convection	105.2	122.8	48.6	60.1
Std. dev.	13.5	18.4	3.2	2.8
VFM	68.5	108.6	29.5	50.4
Std. dev.	14.6	18.0	3.0	3.6
Change	- 35%	- 12%	-39%	- 16%
VFM (DOE)	38	75	18	37
Change (DOE)	- 64%	- 39%	- 63%	- 38%

Thinner Die and Boards

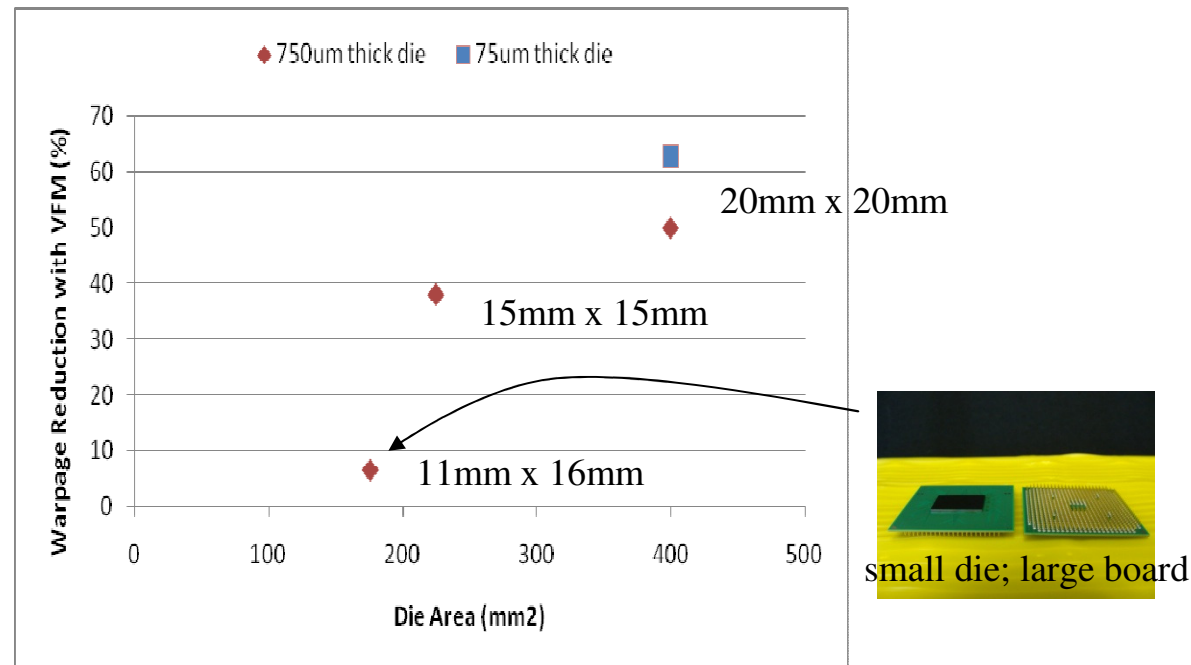
- ❑ New test parts:
 - 20mm x 20mm x 75μm silicon die
 - 47mm x 30mm x 200μm thick BT substrates
 - Same Hybrid UF
- ❑ 4 assemblies each cured by standard convection and VFM
 - Two day sitting time between cure and 3X reflow treatments

Warpage in Microns (by Shadow Moire')

	BT (cured)	BT (2 days)	BT (3X reflows)	Si (cured)	Si (2 days)	Si (3X reflows)
Convection	756.3	668.8	889.8	407.5	355.3	509.3
VFM	263.5	287.3	330.0	204.0	158.8	357.5
Change	- 65%	- 57%	- 62%	- 50%	- 55%	- 30%

Size is a Critical Factor

- ❑ Larger size dice show more improvement with VFM cure



- ❑ Thinner dice/boards show more improvement with VFM cure

Why Expect Lower Warpage from VFM Curing?

1. Uniform heat distribution
2. Low temperature
3. Material-selective heating
4. Morphology/Chemistry

1. Uniform bulk heating decreases warpage

- ❑ Wire-bonded dice with encapsulant ¹
- ❑ Henkel-Loctite EO1072; substrate Ar/O₂ etched; Asymtek dispenser

	Cure (%)	Warpage
Convection 145C / 70 min	99.9	3.5 mm
VFM 100C/3min + 120C/4min	99.9	<< 0.5 mm

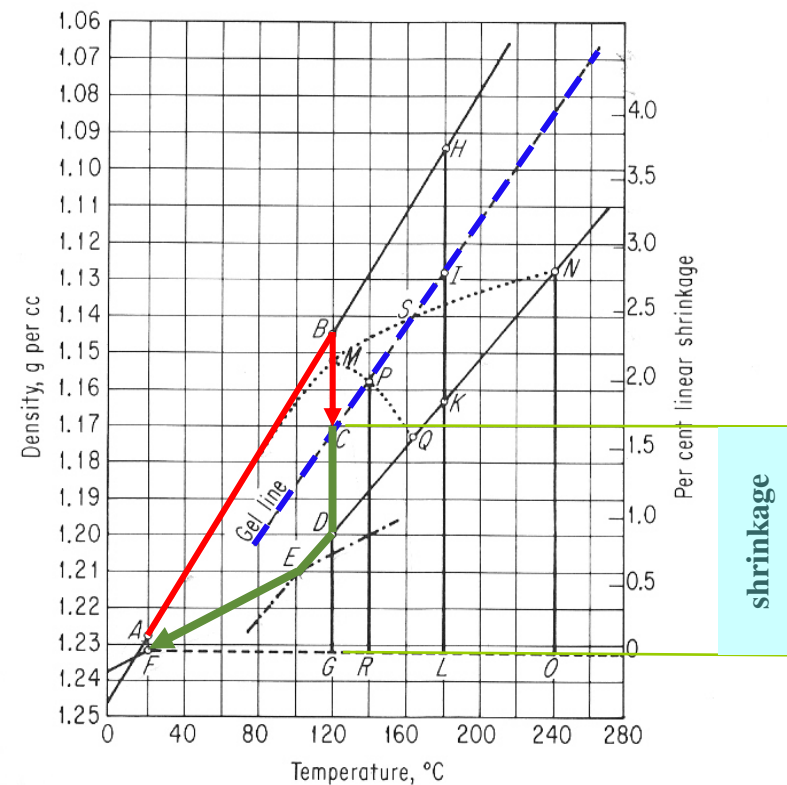
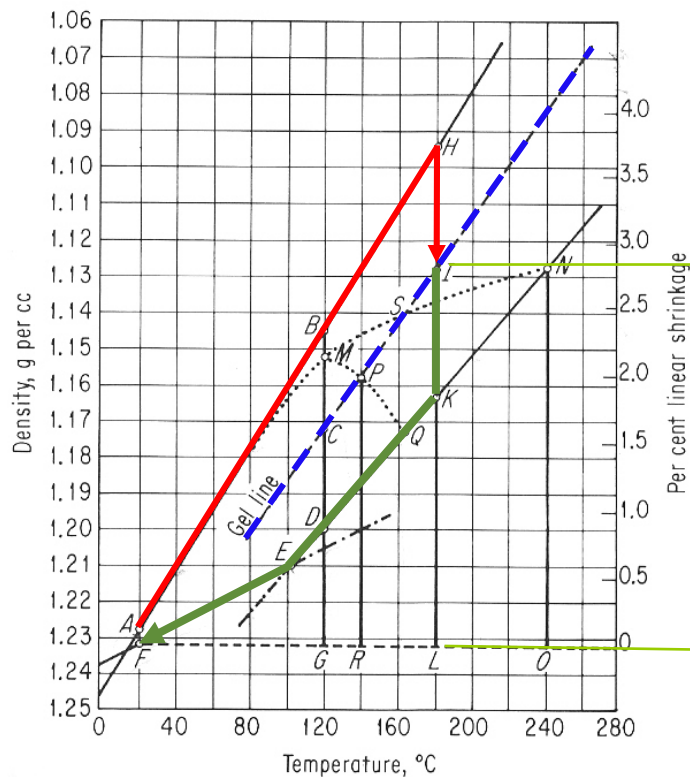


- ❑ Wafer films (10-20 μm) show 50% lower warpage ² (at same T_g)

1. Hubbard et.al., International Microelectronics and Packaging Conference, October, 2006.
2. Hubbard et.al., International Wafer Level Packaging Conference, October, 2009.

2. Lower Stress from Lower Temperature Cure

- VFM can lower cure temperature profile by 30-200°C
- UF cure of 115°C / 6 min. compared to 145°C / 120 min.
- Ramp rates of 30°/sec rather than 3°/sec



Reference: Lee and Neville, Handbook of Epoxy Resins, McGraw-Hill, NY, 1967.

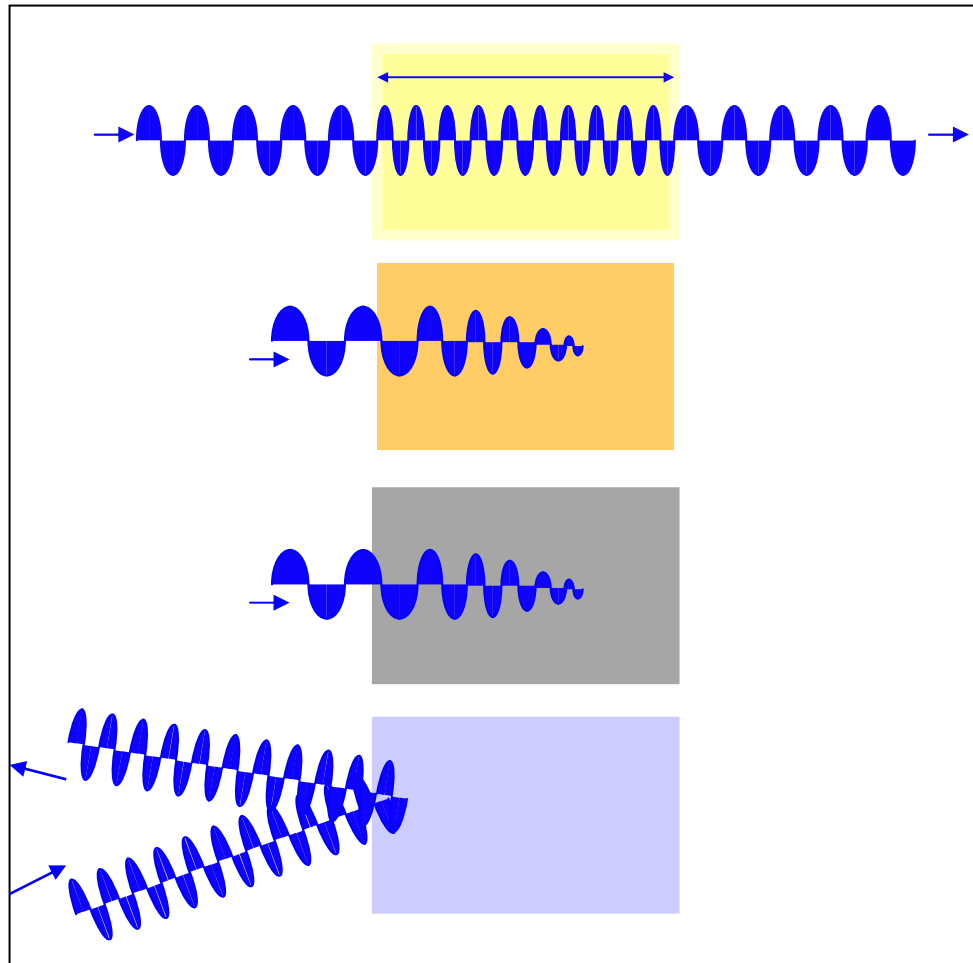
3. Selective Heating

□ Glass & Ceramics

□ Polymer resins

□ Silicon (doped)

□ Metals



transparent

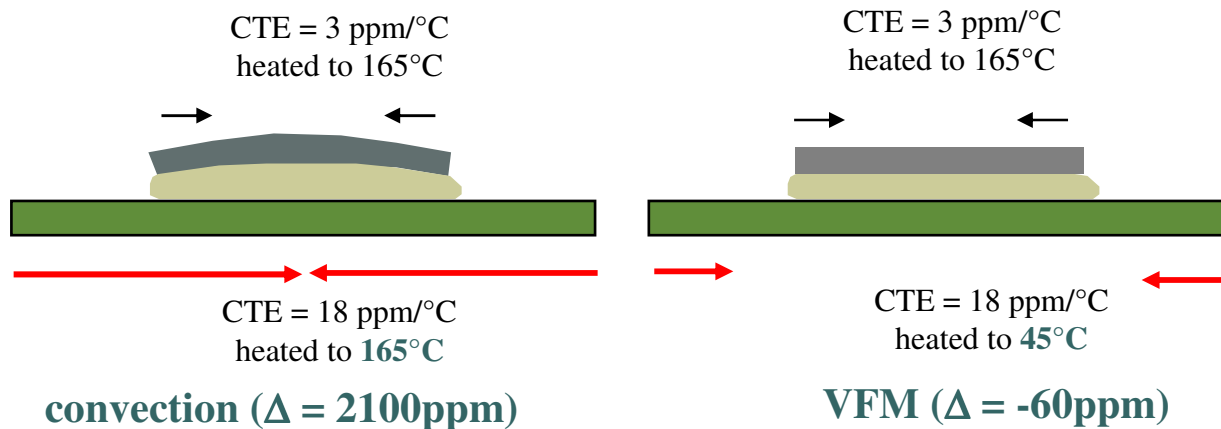
absorptive

absorptive

reflective +
absorptive +
transparent

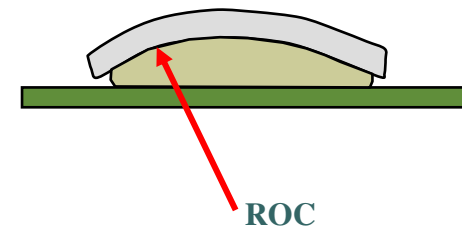
3. Selective heating with VFM

- ❑ CTE mis-match: compensated for with VFM by selective heating
 - VFM doesn't heat the board or other components



- ❑ Lower warpage (higher radius of curvature) and stronger adhesion

	Push-off (psi)	ROC (in)
Convection 150C/120min	986	48
Convection 100C/60min + 150C/120min	1069	53
VFM 130C/2min + 150C/2min	1620	299

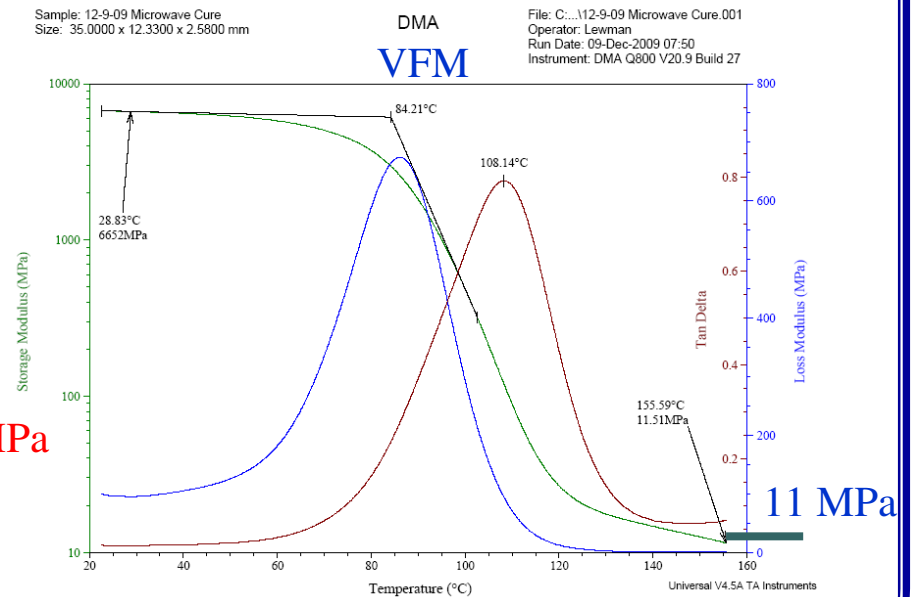
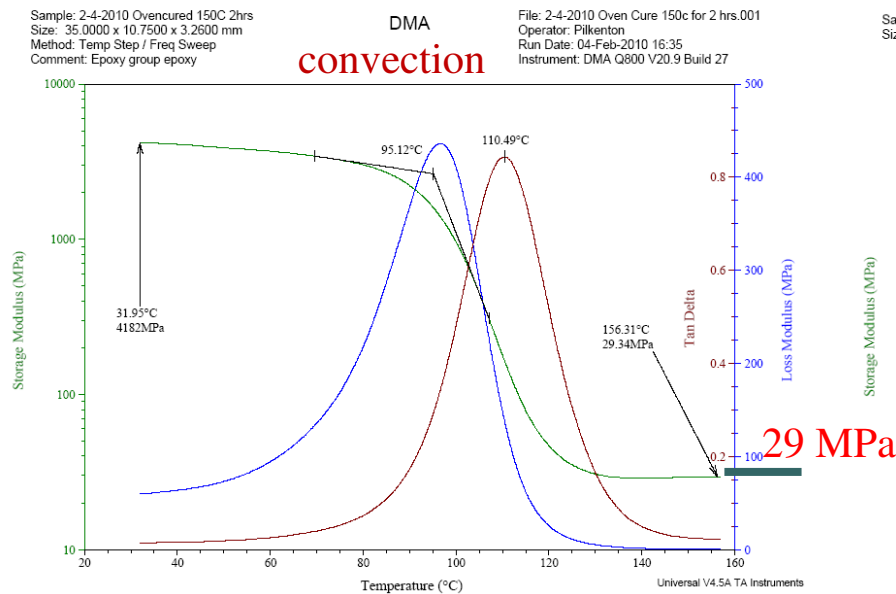


References: Fathi et.al., *Circuits Assembly*, July 1998.
 Anderson, et.al., *Proceedings NEPCON West*, 1998.

4. Lowered E' with VFM Cure

□ Hybrid UF Material (above)

- Cured to the same T_g (see tanδ peak in red)
- Elastic (storage) modulus is lower above the T_g
- This indicates a more flexible cross-linked network: lower stress



Conclusions and Directions

- ❑ Reduced warpage of flip-chip under-fill assemblies with VFM cure
 - Effects are in addition to optimized convection oven profiles
 - Consistent with previous studies and production results
- ❑ Lowered stress is permanent
 - 260°C Solder reflow cycles do not reset thermo-mechanical properties
- ❑ Lower temperature cure and faster cycle time additional benefits
- ❑ VFM cure profiles can be optimized for board or die co-planarity
 - If no BGA reflows necessary, much lower warpage remains
- ❑ Warpage reduction not specific to under-fill chemistry
- ❑ Consistent results with live FC assemblies.
- ❑ Further evaluations of commercial UF materials
 - Find the lowest possible warpage cure profiles for existing UF
 - Optimize for material compositions and adhesive types